Multi Layer Graphene Nano-Ribbon Interconnects Based Driver-Interconnect-Load System

P. Agnihotry and R.P.Agarwal

***Abstract*—Nowadays planar graphene based interconnects known as graphene nano-ribbons (GNR), are used for interconnections in VLSI and ULSI chips. The form of GNR which is widely used is multi layer graphene nano-ribbon (MLGNR). In this paper study of propagation delay of a driver-interconnect-load system (DIL) has been carried out along with MLGNR beyond 16nm and comparison has been made with the DIL systems used at 16 nm. In this work different numbers of devices that are connected in parallel have also been considered for three different operating regions like super threshold region, near threshold region, and sub threshold region.**

***Index Terms*—FinFET, Interconnects, Multi layer graphene nano-ribbon, propagation delay.**

I. Introduction

Graphene is a two dimensional planar VLSI interconnects which are widely used because of its superior performance. One of the most important property of graphene nano-ribbon, which makes it popular, is that electrons can move a long distance without being scattered [1-3]. Like carbon nanotube (CNT) graphene nano-ribbon can be classified as conducting and semiconducting depending on the relations, N = 3m − 1 (metallic) or N = 3m, 3m + 1 (semiconducting), where m is an integer and N is the number of hexagonal carbon rings across the width of GNR [4].

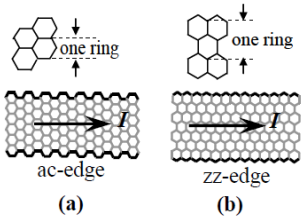

Fig. 1. Schematic view of (a) armchair-GNR and (b) zigzag-GNR[4].

The paper deals with the calculation of propagation delay for a driver-interconnect-load (DIL) system along withmulti layer GNR interconnects in nano scale region and comparison has been carried out between the calculated values of propagation delay at 16 nm and beyond.

Variation of length and width of interconnect has been taken to calculate the delay parameter.DIL system comprises of CMOS, Short-Gate (SG) FinFET, Independent-Gate (IG) FinFET, and Low-Power (LP) FinFET driver and load circuits has been used and GNR which has been used in the system is of multi layer.

II. Method and Methodology

The driver and load circuits which are used in the driver-interconnect-load (DIL) system are CMOS and FinFET. FinFET is a multi-gate device that having wrapped conducting channel under thin silicon (called fin) which forms the body of the device.

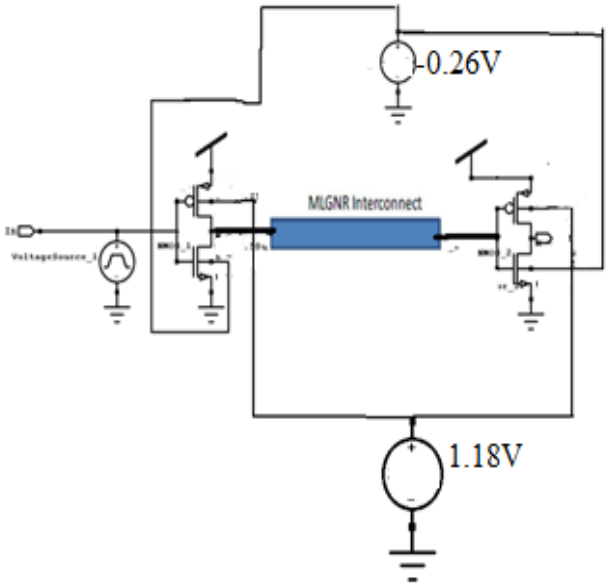

Fig. 2. Driver-interconnect-load system using LP FinFET driver-load

There are three variants of FinFET which have been used, in SG FinFET driver the front and back gates of PMOS and NMOS transistors are connected with each other and IG FinFET driver of n-type has been used in which front and back gates of PMOS transistor are short with each other and back gate of NMOS transistor is providing with another voltage source, and in LP FinFET both gates are at different potentials for PMOS and NMOS transistors [8].

The GNR which has been used is neutral MLGNR with no intercalation doping. For neutral MLGNR the Fermi level which has been used is 0.1eV with 0.34 nm spacing between graphene layers and for neutral MLGNR mean free path is 419 nm [6].

III. Results and Tables

The simulation has been carried out by considering different layers of GNR (3.10, and 20) and having width of layer equal to 10nm, 20nm, 30nm, 40nm up to 100nm. The length of interconnect varied from 100 μm to 1000 μm and

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results have been calculated using TSPICE 14.0.For the case of LP FinFET driver-load circuit the back gate for NMOS transistors are set at -0.26V and back gates for PMOS are adjusted at 1.18V [7].

Agnihotry et. al [5] has been calculated the delay variation with respect to length of interconnect and width respectively at 16 nm. This paper studies the effect beyond 16 nm and comparison has been made with that of 16 nm.

Fig. 3 and Fig. 4 shows the delay variation with length and width of interconnect respectively beyond 16 nm. The number of devices that are connected in parallel has been represented by M and values of M that have been considered are 1, 3, and6.

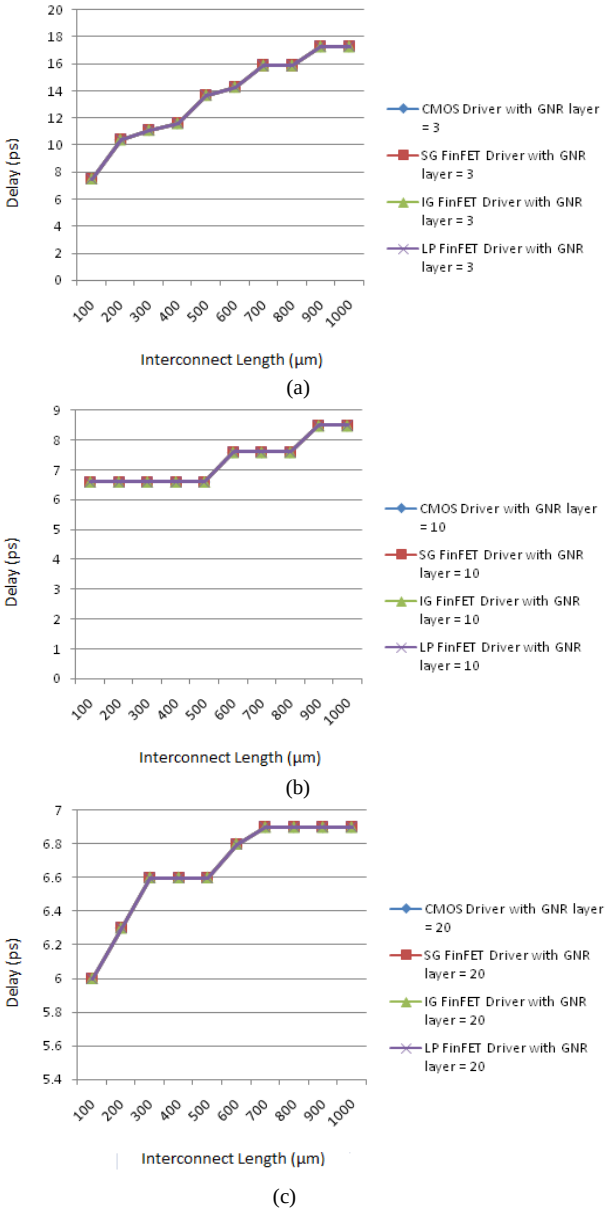


Fig 3. Delay variation of different DIL systems at Vin = 0.5V

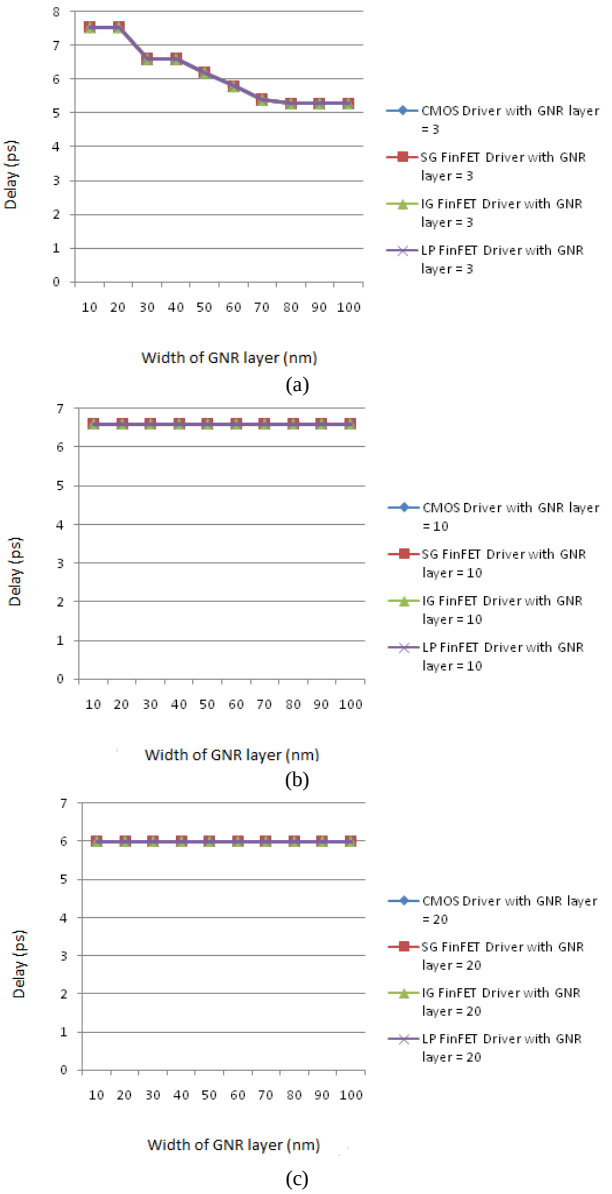
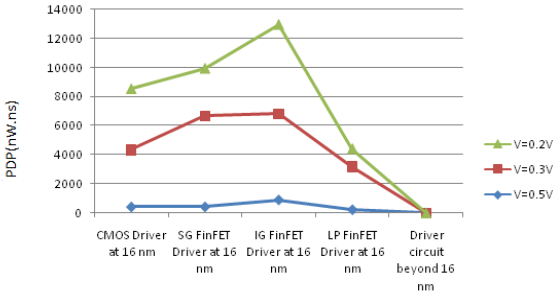
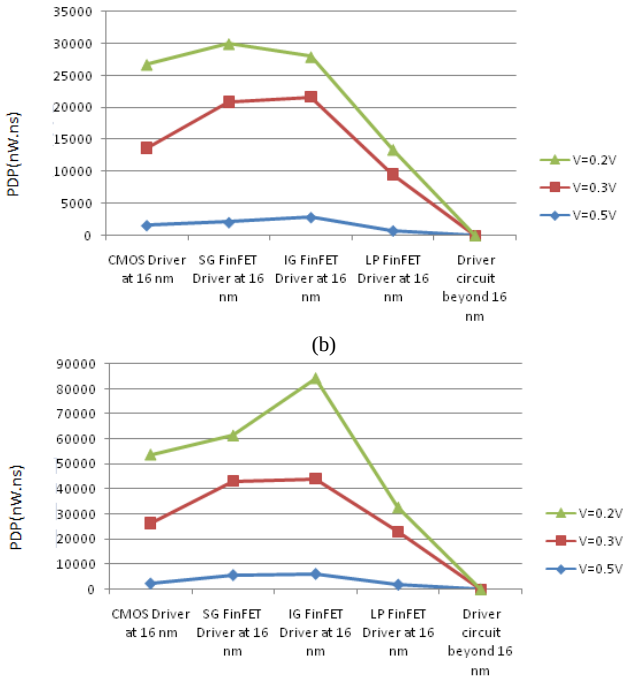


Fig. 4. Effect of width variation of different DIL systems on delay at Vin =0.5V

From the results of Fig.3 and 4 it is clear that there is no change in propagation delay values at driver and load side beyond 16 nm. Therefore one type of driver and load circuit beyond 16 nm has been considered for calculating the improvement percentage of delay of DIL system beyond 16 nm over 16 nm node



(a)



(c)

Fig. 5. Power delay product variation of different DIL systems for (a) GNR layer = 3 and M=1, (b)GNR layer = 3 and M=3, and (c) GNR layer = 3 and M=6

Fig.5 shows the power delay product (PDP) of different DIL systems at 16 nm and beyond. From the results it is clear that the PDP of DIL system used beyond 16 nm shows very small value because for DIL systems using at 16 nm delay is in nano-seconds (ns) and for DIL system beyond 16 nm delay is of the order of pico-seconds (ps).

TABLE I: PERCENTAGE IMPROVEMENT OF PROPAGATION DELAY OF DIL SYSTEM BEYOND 16 NM OVER 16 NM NODE FOR GNR LAYER = 3

% improvement of delay at GNR layer = 3									
Vin	0.5V			0.3V			0.2V		
	M=1	M=3	M=6	M=1	M=3	M=6	M=1	M=3	M=6
CMOS DIL	99.5	99.5	99.5	98.8	98.8	98.8	99.6	99.6	99.6
SG FinFET DIL	99.4	99.5	99.5	98.8	98.8	98.8	99	99	99
IG FinFET DIL	99.7	99.6	99.6	99	99	99	99.7	99.7	99.7
LP FinFET DIL	99.7	99.6	99.6	99.7	99.7	99.8	99.9	99.9	99.9

TBLE II: PERCENTAGE IMPROVEMENT OF PROPAGATION DELAY OF DIL SYSTEM BEYOND 16 NM OVER 16 NM NODE FOR GNR LAYER = 10.

% improvement of delay at GNR layer = 10									
Vin	0.5V			0.3V			0.2V		
	M=1	M=3	M=6	M=1	M=3	M=6	M=1	M=3	M=6
CMOS DIL	99.5	99.6	99.7	98.8	98.8	98.8	99.6	99.6	99.6
SG FinFET DIL	99.4	99.6	99.7	98.8	98.8	98.8	99	99	99
IG FinFET DIL	99.7	99.7	99.7	99	99	99	99.7	99.7	99.7
LP FinFET DIL	99.7	99.7	99.7	99.7	99.7	99.8	99.8	99.8	99.8

TABLE III: PERCENTAGE IMPROVEMENT OF PROPAGATION DELAY OF DIL SYSTEM BEYOND 16 NM OVER 16 NM NODE FOR GNR LAYER = 20

% improvement of delay at GNR layer = 20									
Vin	0.5V			0.3V			0.2V		
	M=1	M=3	M=6	M=1	M=3	M=6	M=1	M=3	M=6
CMOS DIL	99.5	99.6	99.7	98.8	98.8	98.8	99.5	99.6	99.6
SG FinFET DIL	99.5	99.6	99.6	98.8	98.8	98.8	99	99	99
IG FinFET DIL	99.7	99.7	99.7	99	99	99	99.6	99.7	99.7
LP FinFET DIL	99.8	99.7	99.7	99.6	99.7	99.8	99.8	99.8	99.7

IV. CONCLUSION

From the results which have been found in the paper it has been concluded that performance of the DIL systems beyond 16 nm in terms of propagation delay is practically same. The improvement percentage in delay has been shown in the paper which shows that the DIL system when used beyond 16 nm give better improvement in speed in comparison with the DIL system used at 16 nm.

Also from power delay product (PDP) graph it is clear that the PDP of DIL system used beyond 16 nm is very small as compared to that used at 16 nm. From the calculated results it has been concluded that the DIL system comprises of FinFET and MLGNR is a good candidate for the nano scale region in terms of speed and power dissipation. Therefore, for the future VLSI and ULSI chips this proposed DIL system will show superior performance.

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